REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 1-21 are pending. Claim 1 is currently amended to more clearly define pre-existing claim limitations. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

Claim 1 stands rejected under 35 U.S.C. §112, second paragraph for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,911,640 to Bencuya et al. (hereinafter "Bencuya") in view of U.S. Patent No. 6,163,023 to Watanabe (hereinafter "Watanabe").

Claims 7-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe in view of Bencuya.

Claims 1-21 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of copending Application No. 10/752,112.

Response to Rejections under 35 U.S.C. § 112, second paragraph

The Office Action rejection claim 1 under 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully submits that claim 1, as amended, more clearly defines pre-existing claim limitations. Applicant also respectfully notes that claim 1 does not include specific references to hard and soft resets. Accordingly, Applicant

respectfully requests that the rejection of claim 1 under 35 U.S.C. §112, second paragraph be withdrawn.

Response to Rejections under 35 U.S.C. § 103(a)

The Office Action rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over Bencuya in view of Watanabe. Applicant respectfully requests withdrawal of these rejections because the Office Action has failed to establish a prima facie case of obviousness and the combination of cited references does not teach or suggest all of the limitations of the claim.

CLAIMS 1-6

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bencuya in view of Watanabe. Applicant respectfully submits that claim 1 is patentable over the combination of cited references because the Office Action has failed to establish a prima facie case of obviousness and the combination of cited references does not teach or suggest all of the limitations of the claim. Claim 1 recites:

> A circuit for a pixel site in an imaging array, comprising:
> a pixel to convert incident light to an electrical signal;
> a row line to read out a voltage from said pixel;
> **a row line transistor, operatively connected between one end of said row line and a predetermined voltage, to reset a voltage associated with said row line;** and
> a reset voltage generator, operatively connected to said row line transistor, to
> generate reset pulses;
> **said reset voltage generator generating a first reset pulse at a beginning of an integration period of said pixel;**
> **said reset voltage generator generating a second reset pulse after generating said first reset pulse, the generation of the second reset pulse being at an end of the integration period of said pixel.** (Emphasis added).

Applicant respectfully submits that claim 1 requires a row line transistor between one end of a row line and a predetermined voltage to reset a voltage associated with said row line, and that that the reset voltage generator generates a first reset pulse at a beginning of an integration period and a second reset pulse after the first reset pulse. The cited combination fails to disclose at least this limitation of claim 1.

Bencuya is directed to CMOS image sensor having a reset transistor, a photodiode, reset drain voltage circuitry, and rest gate voltage circuitry. Bencuya, Abstract. During the reset operation, the reset drain voltage circuitry supplies a first drain voltage to the drain of the reset transistor in accordance with a determined level of light for exposure to perform a "hard reset." Bencuya also discloses that the hard reset is immediately followed by a "soft reset." Bencuya, Abstract. As illustrated and described with respect to Figures 5 and 6, Bencuya discloses the "hard reset" occurs between time t0 to time t1, and the "soft reset" occurs between time t1 and time t2. Bencuya, col. 7, line 63 to col. 8, line 44. However, as correctly pointed out in the Office Action, nothing in Bencuya discloses that the reset voltage generator generates a second reset pulse after generating the first reset pulse. Office Action, mailed May 11, 2007, pages 4.

The Office Action, however, purports that Watanabe teaches this limitation, and that it would be obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bencuya, which teaches a reset pulse by adding a second reset pulse after a period of time. Office Action, mailed May 11, 2007, page 4. Applicant respectfully submits that claim 1 is patentable over the combination of cited references because the Office Action has failed to establish a prima facie case of obviousness and the combination of cited references does not teach or suggest all of the limitations of the claim.

Applicant respectfully submits that the Office Action has failed to establish a prima facie case of obviousness regarding the combination of the cited references because the Office Action has only made a *conclusory statement* that it would have been obvious to modify Bencuya's teaching with the teachings of Watanabe to generate a second pulse after a period of time because the pulses need to be repeated to go through all the pixel sites, without explaining what specific understanding or technological principle within the knowledge of one of ordinary skill in the art would have prompted one of ordinary skill in the art to combine the elements in the manner claimed. See Memorandum from Deputy Commissioner, May 3, 2007, regarding Supreme Court decision on *KSR Intl'l Co., v. Teleflex, Inc.* Here, the Office Action merely states that in order to go through all the pixel sites, the pulses (as described with respect to one pixel site) are repeated, without explaining what specific understanding or technological principle within the

knowledge of one of ordinary skill in the art would have been prompted them to combine the elements in the claimed manner.

Moreover, even if a person of ordinary skill in the art would have been prompted to combine the cited references, the combination of cited references stills fail to disclose all the limitations of claim 1. In particular, the combination of cited references fail to disclose a row line transistor, operatively connected between one end of said row line and a predetermined voltage, to reset a voltage associated with said row line.

As set forth in the Office Action, the Office Action purports that Bencuya discloses a row line transistor, operatively connected between one end of said row line and a predetermined voltage, to reset a voltage associated with said row line. Office Action, mailed May 11, 2007, page 3. Applicant respectfully disagrees with the Office Action's characterization of the cited reference.

Bencuya discloses a CMOS image sensor having an array of active pixel sensor, represented by active pixel sensor 102, illustrated in Figure 1. Bencuya, col. 3, lines 17-19. The active pixel sensor 102 a photodiode, a reset transistor, a source follower transistor, and a select transistor. The reset transistor is connected to the reset drain voltage circuitry (as well as to the drain of the source follower) at its drain, to the photodiode at the source, and to a reset gate voltage circuitry at the gate. Bencuya, col. 3, lines 19-27. The source of the read transistor is connected to its associated column bus at node 124, and receives a read select signal to activate the read transistor during a read operation of the pixel. The Office Action has interpreted the column bus to be the row line upon which a voltage is read from the pixel. Office Action, mailed May 11, page 3. Even interpreting the column bus to be the row line upon which a voltage is read out from the pixel, nothing in Bencuya discloses a row line transistor coupled to the row line of the pixel and a predetermined voltage. Although Bencuya discloses a reset transistor, the reset transistor 106 of Bencuya *does not constitute a row line transistor*, because, first, it is part of the pixel sensor 102 (see Figure 1), and second, it is not *operatively connected between one end of the row line and a predetermine voltage,* and does not reset a *voltage associated with the row line* because the reset transistor 106 is connected to the reset drain voltage circuitry, the photodiode, and the reset gate voltage circuitry, not between the column bus 124 and a predetermined voltage. As such, Bencuya fails to disclose at

least this limitation of the claim. Watanabe fails to cure the deficiency of Bencuya. Accordingly, the cited combination fails to disclose all the limitations of claim 1.

Given that the Office Action has failed to establish a prima facie case of obviousness and that the combination of the references would still fail to disclose all of the limitations of claim 1, Applicant respectfully submits that claim 1 is patentable over the cited references. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 2-6 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 2-6 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 2-6 under 35 U.S.C. § 102(e) be withdrawn.

CLAIMS 7-14

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe in view of Bencuya. Applicant respectfully submits that claim 7 is patentable over the combination of cited references because the Office Action has failed to establish a prima facie case of obviousness and the combination of cited references does not teach or suggest all of the limitations of the claim.

Applicant respectfully submits that claim 7 is patentable over the combination of cited references because the combination of cited references does not teach or suggest all of the limitations of the claim. Claim 7 recites:

> A method for measuring a pixel voltage using a row line, comprising:
> (a) hard resetting the **row line voltage** to a first predetermined voltage;
> (b) soft resetting the row line voltage to a first pixel voltage;
> (c) hard resetting the row line voltage to a second predetermined voltage;
> (d) soft resetting the row line voltage to a second pixel voltage; and
> (e) determining a difference between the first and second pixel voltages, the difference being the measured pixel voltage. (Emphasis added).

Applicant respectfully submits that claim 7 requires hard resetting **a row line voltage** twice and soft resetting the row line voltage twice. The cited combination fails to disclose at least these limitations of claim 7.

Watanabe discloses a pixel read operation in which a signal RS is applied to the reset clock line to discharge the charge stored on the photodiode, thereby

resetting the photodiode. An amplified signal, which is interpreted to be the pixel voltage, is read out to the signal line 13 to obtain the first and second output signals. As such, the row line voltage is read from the pixel at signal line 13 in Watanabe. However, Watanabe discloses that the reset transistor, which receives the RS signal, resets the photodiode, not the signal line 13, which has been interpreted as being the row line. As such, nothing in Watanabe discloses hard resetting the row line voltage to a first predetermined voltage or a second predetermined voltage, or soft resetting the row line voltage to a first pixel voltage or a second pixel voltage.

Bencuya fails to disclose the deficiency of Watanabe. Bencuya does not disclose that the column bus at node 124 is reset, either by a hard reset or a soft reset. Bencuya only disclose that during a hard reset, the reset transistor 106 is turned on and the diode potential rises until the current flow is shut off at the equilibrium potential for the channel. Bencuya, col. 3, lines 54-57. In contrast, during a soft reset, the channel potential of reset transistor 106 and of photodiode are rapidly set to the same level by apply the same potential Vg and Vd of reset transistor 106, causing Vt of reset transistor 106 to increase and slow conduction as the channel of transistor 106 is gradually shut off. Bencuya, col. 4, line 59 to col. 5, line 2. As such, Bencuya does not disclose hard resetting or soft resetting the row line voltage, but only hard and soft resetting the voltage on the photodiode using the reset transistor 106. Accordingly, the combination of cited references fails to disclose all the limitations of the claim.

Given that the combination of the references fails to disclose all of the limitations of claim 7, Applicant respectfully submits that claim 7 is patentable over the cited references. Accordingly, Applicant requests that the rejection of claim 7 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 8-14 depend from independent claim 7, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 8-14 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 8-14 under 35 U.S.C. § 102(e) be withdrawn.

CLAIMS 15-21

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe in view of Bencuya. Applicant respectfully submits that claim 15 is patentable over the combination of cited references for similar reasons described above with respect to claims 1 and 7. In particular, neither Watanabe nor Bencuya discloses a row line including a row line transistor as described above with respect claim 1. Given that the combination of the references fails to disclose all of the limitations of claim 15, Applicant respectfully submits that claim 15 is patentable over the cited references. Accordingly, Applicant requests that the rejection of claim 15 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 16-21 depend from independent claim 15, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 16-21 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 16-21 under 35 U.S.C. § 102(e) be withdrawn.

Response to Provisional Rejections on the Grounds of Nonstatutory Obviousness-type Double Patenting

The Office Action rejected claims 1-21 as being unpatentable over claims 1-21 of copending Application No. 10/752,112. Applicant respectfully submits that a terminal disclaimer is filed herewith in compliance with 37 CFR 1.231(c). Accordingly, Applicant respectfully requests withdrawal of the provisional rejection to claims 1-21 on the grounds of nonstatutory obviousness-type double patenting.

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Daniel Ovanezian at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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